Digitally-Assisted Linearization of Wideband Direct Conversion Receivers

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***Abstract*— A SAW-less direct-conversion receiver is presented which utilizes a mixed-signal feedforward path to regenerate and equalize IM3 products, thus accomplishing system-level linearization. The receiver system performance is dominated by a custom integrated front end realized in 130nm CMOS and achieves an uncorrected out-of-band IIP3 of -7.1dBm under the worst-case UMTS FDD Region 1 blocking specifications. IM3 equalization results in an effective IIP3 of +5.3dBm and reduces total input-referred error by over 23dB.**

I. Introduction

Improving the linearity of RF receivers has long been a challenging circuit design problem. As supply voltages drop with process scaling and as market demands continue to press for the elimination of off-chip components, such as SAW filters, standard techniques for meeting receiver linearity specifications will become inadequate. Direct conversion receivers are of considerable interest in this regard, as they constitute the dominant architecture in modern communication systems. Much progress has recently been made in improving the IIP2 of such circuits; however, a great need still exists to improve upon the IIP3 performance. This paper discusses the concept and details behind a system-level approach to satisfy this need.

II. System-Level Concepts

A. System-Level Linearization via Equalization

In order to improve the system IIP3 for a SAW-less direct-conversion receiver, the original main path of the receiver is augmented with an alternate receiver path, as shown in Fig. 1 below.

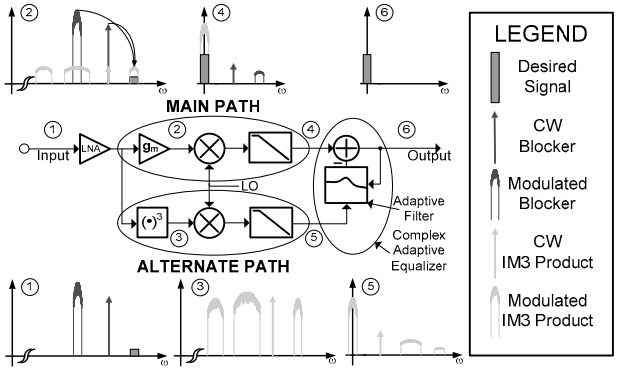

Fig. 1 IM3 equalization concept.

The alternate path generates IM3 products in the analog domain at RF and downconverts them to baseband using the same LO frequency as the main path receiver. The IM3 products are then digitized and are used as inputs to an equalizer which cancels the baseband IM3 products in the main path. Hence, a linearization via equalization is accomplished. Generating the IM3 products after the LNA at RF is a crucial feature of this architecture, since it is at this point in the system that the blocker magnitudes are at their largest.

This solution has the advantages of being both power-efficient and robust. Since the alternate path must pass only IM3 products, the dynamic ranges of its constituent blocks can be over 10dB less than in the main path, allowing for significant power savings in its overall design. As problematic blocker conditions occur roughly less than 10% of the time, the time-averaged power dissipation of the alternate path is further reduced by powering it on only when needed. The adaptive nature of the equalization guarantees robustness in the presence of changes in temperature, LO frequency, and blocker characteristics.

The idea of adaptively cancelling IM3 products has recently been described in a system-level study [1], where the alternate path resides completely within digital baseband. For IM3 cancellation to occur in this scheme, the ADCs must digitize all possible IM3-producing blockers. For example, in FDD UMTS Region 1 this requires digitizing frequency bands from 1670-1850MHz, 2015-2075MHz, and 1920-1980MHz (TX band), rendering this scheme unattractive from a power efficiency perspective. In order to overcome this issue, the mixed-signal approach proposed in this work passes only the problematic IM3 products through the alternate path ADCs. Hence, the alternate path ADC and digital baseband sampling rate requirements are no greater than those of the original main path.

B. Receiver System Architecture

The receiver system architecture described in this paper is shown below in Fig. 2. In order to provide a quantitative design objective, the design targets the FDD UMTS Region 1 standard, as it is well known for its linearity challenges. It contains a custom-designed integrated front-end in 130nm CMOS, analog baseband circuitry on PCB, and a digital back end implemented on an FPGA platform.

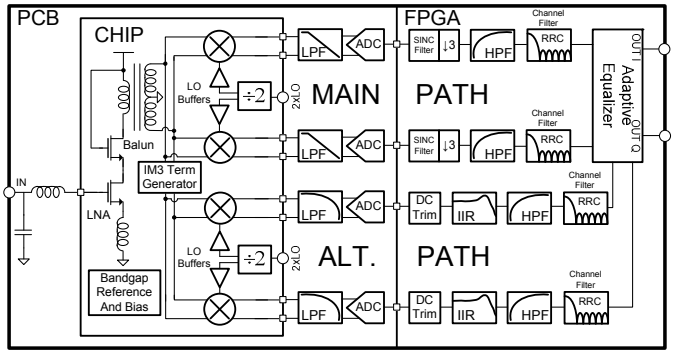

Fig. 2 Experimental UMTS receiver architecture.

Although it is possible to perform the adaptive equalization in analog circuitry, shifting as much of the signal processing burden as possible to the digital domain affords several advantages. For example, the behaviour of digital circuitry is relatively insensitive to process variations, and the continued scaling of digital processes has made baseband digital blocks power-competitive with equivalent blocks in the analog domain.

Considerations specific to modern cellular receivers also factor into the choice of predominantly digital equalization. For example, such receivers often implement adjacent channel rejection filters in the digital domain. To ensure that large adjacent channel signals do not interfere in the adaptive equalization, it is best to place the adaptive equalizer after these filters in the digital domain as well.

III. Analog Circuit Descriptions

A. Main Path Circuitry

As shown in Fig. 2, the LNA is an inductively degenerated cascode architecture which is terminated by a transformer balun. This balun serves as the LNA load inductor and subsumes the single-ended-to-differential conversion previously handled by the interstage SAW filter. The balun is followed by high-IIP2 mixers [2] which are folded in order to function under the 1.2V supply voltage. This choice obviates any IM2 equalization and allows the design effort to focus solely on IIP3 improvement. A frequency divide-by-two circuit which generates I and Q LO phases is also included on chip in order to minimize LO coupling into the substrate and chip ESD guard ring.

The main path baseband circuitry is implemented with discrete, commercially available components. The baseband low-pass filter is a third order Chebyshev architecture and is followed by an 8-bit pipelined ADC running at 50MHz.

B. Alternate Path Circuitry

The alternate path is a low-power, low-area variant of the main path, with the primary difference being the inclusion of an IM3 term generator. In order to conserve area, the alternate path mixer dispenses with the tuning inductor present in the main path mixer. Another I/Q generating frequency divider is used for the alternate path, as routing LO signal from the main path frequency divider increases the risk of LO coupling to other blocks in the system.

Like the main path, the alternate path baseband circuitry is implemented with discrete components. The alternate path baseband low-pass filter is a single real-pole embedded into the ADC buffer, which drives an 8-bit pipelined ADC running at 16.66MHz. Along with the free real pole at the output of the mixer, this level of postfiltering is sufficient to attenuate any IM3 products not involved in baseband equalization to below the alternate path noise floor.

IV. IM3 Term Generator

The IM3 term generator is an unconventional block, and as such, it merits additional consideration in its design. A pure cubing circuit is desired, as it passes negligible linear terms. If present, these terms will be treated as error by the adaptive equalizer, potentially degrading the receiver small signal gain, IM3 correction ratio, or both. Unlike other approaches that utilize the third-order Taylor series coefficient of the MOSFET [3], the design concept used for this IM3 term generator, shown below in Fig. 3, exploits the stronger second-order term by distributing the cubing between a conventional MOS squaring circuit and a Gilbert multiplier. The circuit schematic itself is shown in Fig. 4.

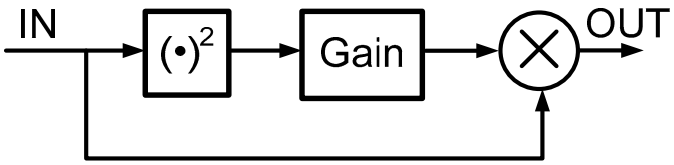

Fig. 3 Multistage cubing concept.

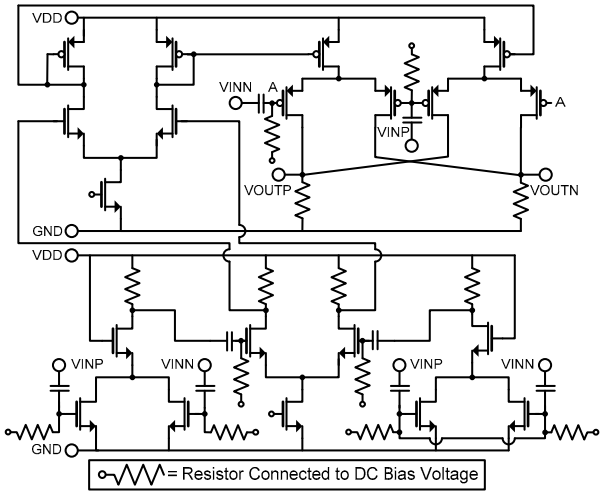

Fig. 4 IM3 term generator schematic.

As it produces a single-ended output, the squaring circuit must be followed by an active balun. To improve the generator CMRR, the negative terminal of the balun is tied to a replica squaring circuit whose gate terminals are shorted. This branch only generates common mode signal, which is then rejected by the CMRR of the balun.

Perhaps the most important aspect of the proposed IM3 term generator is the multistage nature of the cubing. Only the beat frequency terms of the squaring are required to be retained in order to complete the cubing operation. Hence, the

bandwidth of the inter-multiplication circuitry can be substantially smaller than the RF frequencies of the blocker signals, as depicted in Fig. 5 below. In this case, the gain-bandwidth principle can be used to the designer's advantage, as substantial gain can be applied for less power than if the full IM2 spectrum up to 4GHz were retained in between nonlinear operations.

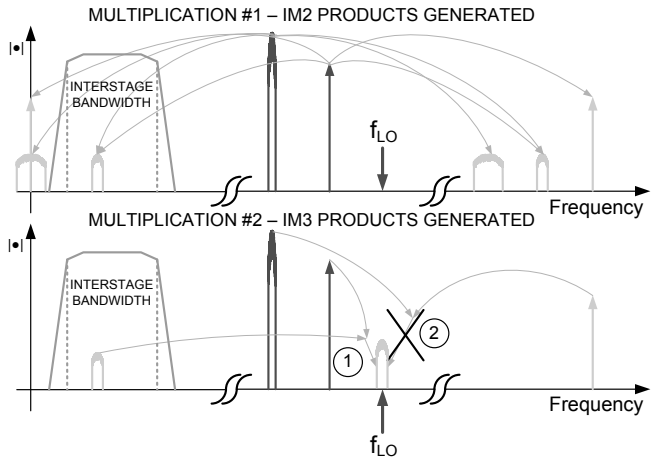

Fig. 5 Multistage cubing: frequency domain considerations.

V. Digital Equalization

The path equalization implemented in this project is performed in the digital domain and is partitioned into fixed and adaptive portions. This choice stems from the fact that the minimal analog postfilters of the main and alternate path were found to be different in both type and order. Adaptive equalization of such a known IIR path difference is computationally inefficient. Therefore, the fixed equalization consists of a three-multiplier IIR filter in the alternate path. The remaining difference between the two paths is a complex DC gain and a small random mismatch in the baseband transfer function. This difference is broadband in the frequency domain and by the duality principle corresponds to a small number of FIR taps required in the adaptive equalizer.

The normalized LMS (NLMS) algorithm was chosen for the adaptive equalization scheme due to its simplicity and convergence speed. The division associated with this algorithm can be log2-quantized, allowing the use of a barrel shifter as a divider. Although a complex LMS-based algorithm such as NLMS can equalize the phase skew between the main and alternate paths, in general the presence of I-Q mismatch on either path limits the available IM3 cancellation. As shown in Fig. 6 below, an additional degree of freedom in the design was added to overcome this issue by feeding back the complex corrected signal back to independent I and Q taps on each of the incoming alternate path signals.

Yet another consideration is that the performance of the adaptive equalizer is limited in the presence of DC offset. To solve this problem, the proposed design includes high-pass filters in the digital domain and DC offset trimming circuitry in the alternate path. Periodic trimming must be performed prior to the alternate path high-pass filters, or the step response incurred when enabling the digital portion of the alternate path will result in an exponential error transient at the output, prolonging equalizer convergence.

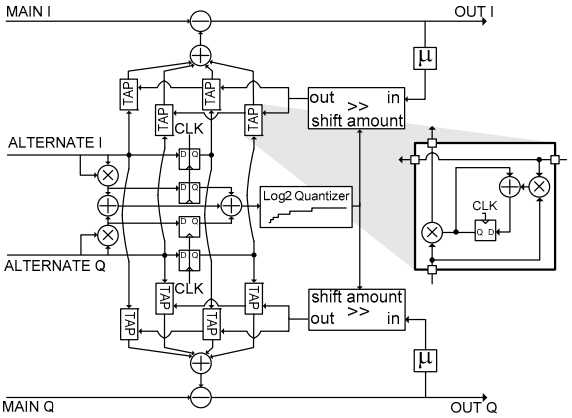

Fig. 6 Enhanced NLMS adaptive equalizer block diagram.

VI. Measurement and Performance

The emphasis of this project is to meet the IIP3 requirements implicitly posed by the UMTS out-of-band blocking test, which must be performed while the TX path is operating at maximum output power [4]. For the duplexer [5], the worst case specified IMD condition, with values referred to the LNA input, is -26dBm TX leakage at 1.98GHz, a -34dBm CW blocker at 2.05GHz, when the receiver LO frequency is set to 2.12GHz. Therefore, under experiment, the receiver is subject to a modified two-tone test, where one of the signals is QPSK-modulated and set to UMTS standards. Accounting for the 2dB loss of the duplexer and the 3dB increase in noise margin allowed under blocking conditions, the maximum allowed total input-referred error is -98dBm [6]. The results of this test are shown in Fig. 7 below and show that in this case under equalization, the input-referred error is -101dBm. (note: here f_{CW}=2.05125GHz, f_{LO}=2.1225GHz) Also shown in Fig. 7 are the results of the same test using the canonical NLMS algorithm. A main path quadrature mismatch of about 3° is partially responsible for the higher input-referred IM3 products.

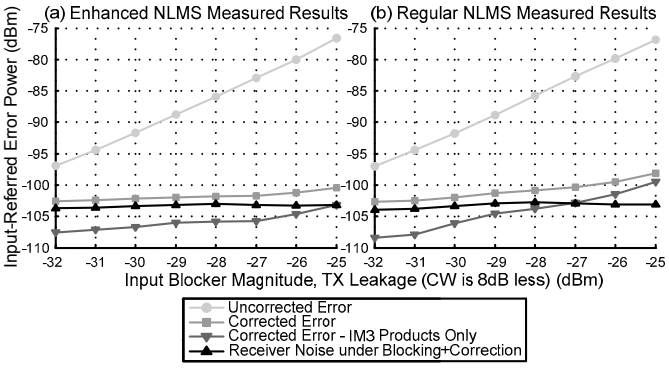

Fig. 7 Measured modified two-tone performance of the receiver, swept over amplitude.

The total input-referred error accounts for gain loss, thermal noise, IM2, and other IM products. Removing the effect of main path thermal noise and IM2 products yields a lumped input-referred quantity consisting of all other error sources. From this quantity, which is treated as residual IM3 error, a slope-of-3 line is extrapolated from the worst-case input blocker magnitude to obtain an effective IIP3 of +5.3dBm. This is an improvement of 12.4dB from the uncorrected IIP3 of -7.1dBm. This test was also performed at all 12 UMTS RX frequencies, with the results of this experiment shown below in Fig. 8. Note that in Figs. 7 and 8, the calculated thermal noise of the 50Ω input impedance is removed to isolate the performance of the receiver circuitry.

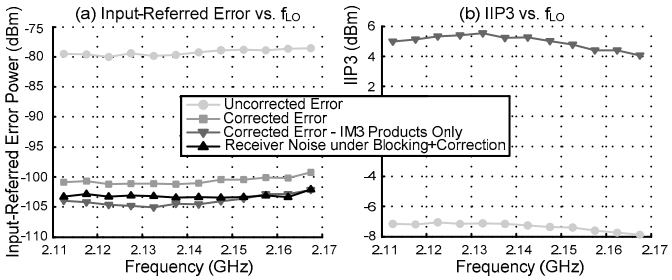

Fig. 8 Measured modified two-tone performance of the receiver, swept over LO frequency. At LNA input TX power is -26dBm, CW power is -34dBm.

Convergence behavior of the adaptive equalizer is shown in Fig. 9 below for the case where the TX leakage amplitude is -25dBm and the CW blocker amplitude is -33dBm at the LNA input at f_{LO}=2.1225GHz.

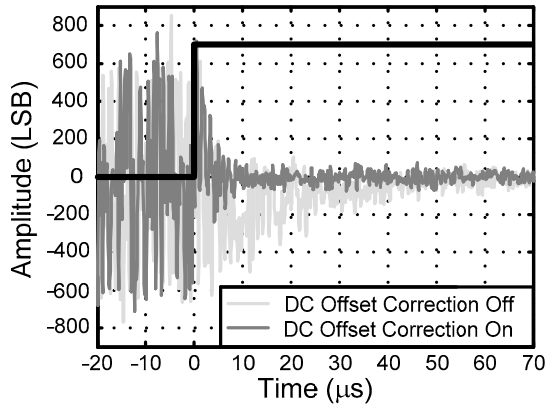

Fig. 9 Measured convergence of the adaptive equalization algorithm.

The measured performance summary of the receiver is shown below in Fig. 10. Fig. 11 shows a die photograph of the integrated RF CMOS front end. Digital power and area numbers are pre-layout estimates derived from a 90nm CMOS standard cell library with estimated wiring parasitics.

VII. Conclusion

This paper describes a UMTS receiver with an integrated front end that cancels IM3 products using a novel mixed-signal feedforward loop. Issues regarding the generation of reference IM3 products, path I-Q mismatches, and DC offset are considered, shown to be relevant, and overcome.

Parameter Measured at f_{LO}=2.1225GHz	Result
Total Active Analog Die Area	1.6mm × 1.5mm
Active Alternate Path Analog Die Area	0.5mm × 0.4mm
Analog Die Technology Node	130nm CMOS
Estimated Digital Alternate Path Area	0.42mm× 0.42mm
Digital Die Technology Node	90nm CMOS
Analog Die LNA+Main Path DC Gain	30.5dB
Complete LNA+Main Path DC Gain to ADC Input	70.2dB
Return Loss (S11) 2.11GHz-2.17GHz	<-13dB
IIP2@1.98GHz	+58dBm
Uncorrected IIP3 @1.98GHz/2.05125GHz	-7.1dBm
Effective IIP3@1.98GHz/2.05125GHz	+5.3dBm
ICP1@1.98GHz	-19dBm
Analog Die LNA+Main Path NF	5.1dB
Complete LNA+Main Path NF	5.5dB
Analog Die Supply Voltage	1.2V/2.7V
Analog Die LNA+Main Path Current	28mA (1.2V)
Analog Die Alternate Path Current	6.7mA (1.2V)
Estimated Digital Alternate Path Current	5.6mA (1.0V)
Baseband Signal Measurement Bandwidth	10kHz-1.92MHz

Fig. 10 Measured performance summary of receiver.

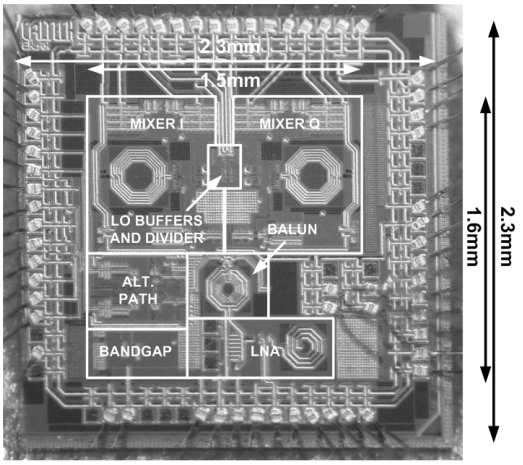

Fig. 11 RF CMOS front-end analog die.

Acknowledgements

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